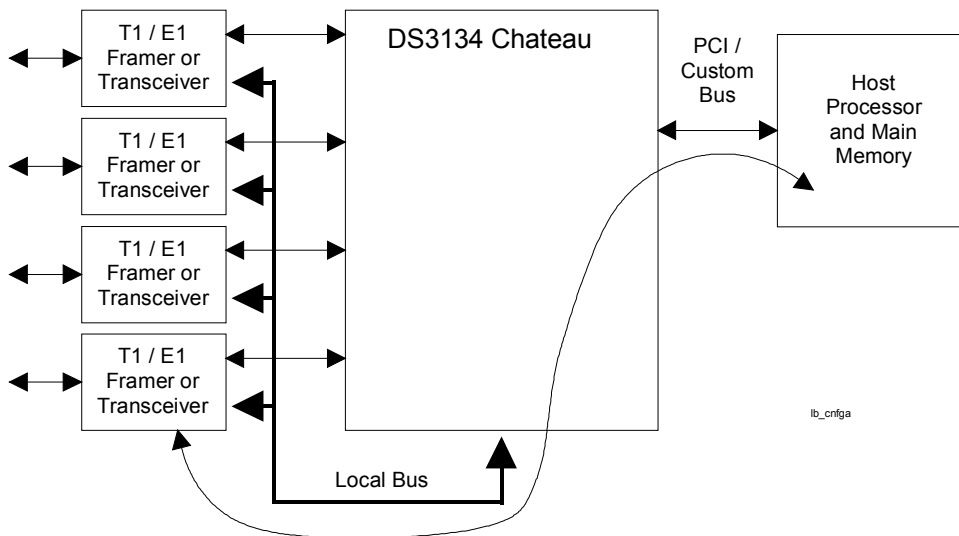


OVERVIEW

This application note describes how to configure the Chateau to configure external devices using the Chateau as a bridge from the PCI bus. Figure 1 is an example of this type of configuration. Also, the datasheet describes more configurations under Section 10: Local Bus. This application note will describe this particular configuration which is the most common.

BRIDGE MODE Figure 1



To use the device in this mode, a few registers must be set:

The PCI local bus memory base address register must be set. This may be set automatically by the host. If the host is a PC, then the operating system will write this register, mapping it in the PCI address space. If it is not automatically set, the user will have to determine where to place it in his own memory map, giving it 1 MB of space.

Offset/ Address	Acronym	Register Name	Data Sheet Section
0110	PLBM	PCI Local Bus Memory Base Address Register	9.2
0104	PCMD1	PCI Command / Status Register 1	9.2

The PCI Command/Status Register 1 must be configured. The MSC bit, bit 1, Memory Space Control should be set to a one to allow accesses to the Local Bus.

The Local Bus Bridge Mode Control Register (LBBMC – 0x40h) must be configured. The user must set whether his local bus will be in 8-bit or 16-bit mode. This is important because if the bus is only 8 bits wide, a user cannot attempt a read or write that is 16 bits. In that case a Target Abort will be issued by the PCI bus. In other words, the user will use a “Write_Byte” procedure for an 8-bit bus, and a “Write_Word” procedure for a 16-bit bus. Also contained in this register is the configuration of the duration of a read or write from/to the local bus, defined in number of LCLKs. The default value (0000) uses the LRDY input to control the length of the bus transaction.

Offset/Address	Acronym	Register Name	Data Sheet Section
0040	LBBMC	Local Bus Bridge Mode Control Register	10.2

For example, if you wanted to configure the DS2155, a T1/E1 transceiver, you could configure the Chateau as follows:

```
PCMD1 = 0x00000002 // MSC – allow access to the Local Bus
LBBMC = 0x0061     // LBW = 8 bit bus, LRDY = 1000 – 8 LCLK periods, LCLKE
```

So if LCLK is 33 MHz, 8 LCLK periods is equal to a local bus access time of 242ns, which works just fine according to the DS2155 parallel port specifications.